

Description

[METHOD OF INCREASING CELL RETENTION CAPACITY OF SILICON NITRIDE READ-ONLY-MEMORY CELL]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92117551, filed June 27, 2003.

BACKGROUND OF INVENTION

[0002] Field of Invention

[0003] The present invention relates to a method of fabricating memory. More particularly, the present invention relates to a method of increasing the data retention capacity of a silicon nitride read-only-memory cell.

[0004] Description of Related Art

[0005] Flash memory is a type of programmable/erasable non-volatile memory. Aside from power down data retention capacity, flash memory also has in-circuit electrical programming and erasing capability. Thus, flash memory is

deployed as a non-volatile memory device inside most personal computers and electronic equipment.

[0006] Flash memory can be classified into two major types, including doped polysilicon floating gate read-only-memory and silicon nitride read-only-memory with the silicon nitride layer serving as a charge-trapping layer. The electrons for injecting into the silicon nitride charge trapping layer of the silicon nitride read-only-memory is concentrated within a localized region.

[0007] For a silicon nitride read-only-memory, data retention period in excess of ten years is often demanded besides the normal reliability requirements in all memory devices. Furthermore, the silicon nitride read-only-memory must operate normally after numerous programming and erasing operations. To meet such stringent conditions, the silicon nitride read-only-memory must undergo a cell retention check during a reliability test. In general, the cell retention check is carried out during a wafer sort test. The check includes heating the finished wafer product to a temperature of about 250°C and maintaining at this temperature for a 24-hour period. During the check, a high voltage is applied to the memory to conduct data programming.

[0008] In the process of fabricating the silicon nitride read-only-memory, the two outermost word lines located on each side of the memory cell array are vulnerable to various types of in process damages, ultimately damaging the tunnel oxide layer. Moreover, some of the steps may require a plasma treatment leading to some holes trapped within the damaged tunnel oxide layer. In a convention fabrication process, the silicon nitride read-only-memory wafers are sorted after conducting a wafer acceptance test (WAT) and a quality control visual inspection. If the wafer is damaged so that the tunnel oxide layer contains trapped holes, these holes may induce the charges within the charge-trapping layer to leak into the substrate through the tunnel oxide layer during a cell retention check. Ultimately, there is a loss of charges leading to a lowering of memory retention capacity and threshold voltage.

SUMMARY OF INVENTION

[0009] Accordingly, one object of the present invention is to provide a method of increasing cell retention capacity of a silicon nitride read-only-memory cell by preventing charges leaking from the charge-trapping layer so that a constant threshold voltage can be maintained.

[0010] This invention also provides a method of increasing cell retention capacity of a silicon nitride read-only-memory such that the silicon-nitride read-only-memory is formed on a wafer. The method includes baking the wafer. The baking process is carried out after a final plasma treatment of the wafer but before wafer sorting.

[0011] Since the wafer is baked after the final plasma treatment of the wafer but before the wafer sorting, any holes trapped inside the tunnel oxide layer in each memory cell are removed.

[0012] Furthermore, with the removal of trapped holes within the tunnel oxide layer of the wafer, hole triggered loss of charges is prevented even if the wafer undergoes a cell retention check thereafter. Ultimately, charge retention capacity of the silicon nitride read-only-memory is effectively increased.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0014] The accompanying drawings are included to provide a further understanding of the invention, and are incorpo-

rated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0015] Fig. 1 is a flow chart showing the steps for increasing cell retention capacity of a silicon nitride read-only-memory cell according to a first preferred embodiment of this invention.

[0016] Fig. 2 is a flow chart showing the steps for increasing cell retention capacity of a silicon nitride read-only-memory cell according to a second preferred embodiment of this invention.

[0017] Fig. 3 is a flow chart showing the steps for increasing cell retention capacity of a silicon nitride read-only-memory cell according to a third preferred embodiment of this invention.

[0018] Fig. 4 is a diagram showing the bias voltage characteristic between a finished wafer product with an 8-hours pre-baking and a finished wafer product with a conventional retention check.

DETAILED DESCRIPTION

[0019] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which

are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0020] Fig. 1 is a flow chart showing the steps for increasing cell retention capacity of a silicon nitride read-only-memory cell according to a first preferred embodiment of this invention. In step S100, a patterned passivation layer is formed over a silicon nitride read-only-memory wafer. The steps for forming the patterned passivation layer includes forming a passivation layer over the entire wafer, forming a patterned photoresist layer and removing a portion of the passivation layer using the photoresist layer as an etching mask. Thereafter, the photoresist layer is removed. The step for removing a portion of the passivation layer includes performing a plasma dry etching operation and the step for removing the photoresist layer includes performing a plasma dry etching operation and a solvent wet strip operation, for example.

[0021] In step S102, an after etch inspection (AEI) of the wafer is performed to check if the patterned passivation layer has the correct pattern.

[0022] In step S104, the wafer is baked to remove holes trapped

within the tunnel oxide layer of the silicon nitride read-only memory. The baking process is carried out, for example, by placing the wafer inside a heating device filled with nitrogen gas, preset to a suitable temperature and heating the wafer for a pre-determined time period. In general, the temperature is set to a temperature between 170°C to 300°C and baked for a period between 8 to 24 hours.

[0023] In step S106, an alloying of the wafer is carried out so that the interfaces between the metallic materials within the silicon nitride read-only-memory has better properties. Furthermore, the interface defects of the tunnel oxide layer is repaired so that the quality of the tunnel oxide layer is improved.

[0024] In step S108, the wafer undergoes a wafer acceptance test (WAT) to find out the wafer yield of the wafer fabrication plant.

[0025] In step S110, a quality control (QC) inspection of the wafer is carried out to determine if there is any visual defects or contamination. In general, the wafer is ready for shipment after passing the quality control inspection.

[0026] In step S112, a series of wafer sort tests on the wafer products is carried out. The wafer sort test including, for

example, a memory cell retention check is carried out within a testing plant. The memory cell retention check includes, for example, heating the wafer to a temperature of about 250°C and maintaining the wafer at that temperature for a 24-hour period. In the meantime, a high voltage is applied to perform a programming operation.

[0027] Fig. 2 is a flow chart showing the steps for increasing cell retention capacity of a silicon nitride read-only-memory cell according to a second preferred embodiment of this invention. The second embodiment differs from the first embodiment in that the baking process is carried out after the alloying process but before the wafer acceptance test. The steps for increasing the cell retention capacity of a silicon nitride read-only-memory are described in the following.

[0028] First, a patterned passivation layer is formed over a silicon nitride read-only-memory wafer (step S200). An after etch inspection of the patterned passivation layer is carried out (step S202). Thereafter, an alloying of the wafer is carried out (step S204) and then the wafer is baked to remove the trapped holes within the tunnel oxide layer (step S206). Afterwards, a wafer acceptance test is performed (step S208) and then a quality control inspection of the wafer is

carried out (step S210). Finally, a series of wafer sort tests (step S212) is performed to sort out the wafer products.

[0029] Aside from the first and the second embodiments, a third method for increasing the memory retention capacity of silicon nitride read-only-memory is possible. Fig. 3 is a flow chart showing the steps for increasing cell retention capacity of a silicon nitride read-only-memory cell according to a third preferred embodiment of this invention. One major difference between the third embodiment and the previous two embodiments is that the baking process is carried out after the wafer acceptance test but before the wafer sorting tests. The steps for increasing the cell retention capacity of a silicon nitride read-only-memory are described in the following.

[0030] First, a patterned passivation layer is formed over a silicon nitride read-only-memory wafer (step S300). An after etch inspection of the patterned passivation layer is carried out (step S302). Thereafter, an alloying of the wafer is carried out (step S304) and then a wafer acceptance test is performed (step S306). The wafer is baked to remove the trapped holes within the tunnel oxide layer (step S308). Afterwards, a quality control inspection of the wafer is carried out (step S310). Finally, a series of wafer sort tests

(step S312) is performed to sort out the wafer products.

[0031] Furthermore, the baking process in the third embodiment can be carried out after the quality control inspection but before the wafer sort tests.

[0032] In the aforementioned steps S104, S206 and S308, baking the wafers at a temperature above 170°C for 8 hours is able to remove the holes trapped within the tunnel oxide layer. In general, there is no specific rule to observe in the baking process and hence the baking temperature and time can be varied according to demand. Furthermore, the heating devices can be various types of furnaces or burn-in oven. Alternatively, ultraviolet light can be used to heat up the wafers. In addition, the same heating device for carrying out the cell retention check can also be used for heating the wafer in the baking process.

[0033] In the aforementioned embodiments, the baking process is carried out after the after etch inspection but before the alloying process, or after the alloying process but before the wafer acceptance test, or after the wafer acceptance test but before the quality control inspection, or after the quality control inspection but before the wafer sort tests. However, this invention is not limited as such. In practice, the main cause for holes to trap inside the tunnel oxide

layer is the plasma treatment. Therefore, performing a baking process anywhere after the last plasma treatment of the wafer (in the embodiment of this invention, the dry etching of the photoresist material in steps 100, 200 and 300) but before the wafer sort tests should be included within the scope of this invention.

[0034] Fig. 4 is a diagram showing the threshold voltage shifted characteristic between a finished wafer product with an 8-hours pre-baking and a finished wafer product with a conventional retention check. In Fig. 4, two outermost word lines (L1 and L32) as well as a central word line L16 within the memory cell array of a finished wafer product with 8-hour pre-baking is compared with the same word lines of a standard finished wafer product (without baking). The vertical axis is the cumulative probability. The letter A represents a word line in a central location with 8-hour baking, the letter B represents a word line in a central location without baking, the letters C & E represent two word lines on each side with 8-hour baking, the letters D & F represents two word lines on each side without baking. According to the results shown in Fig. 4, the bias voltage of the word lines C, E on each side of the wafer with 8-hour baking is considerably bigger than the bias

voltage of the word lines D, F on each side of the wafer without baking.

[0035] The results in Fig. 4 shows that baking is able to maintain an almost constant threshold voltage between the word lines on each side of a finished wafer product and the word lines in a central location. That is, the baking process according to this invention is able to limit the loss of charges from the charge-trapping layer to a minimum and improves the charge retention capacity of the wafer product (the silicon nitride read-only-memory).

[0036] In summary, one major characteristic of the invention of the wafer is the execution of a baking process at a preset temperature for a pre-determined period after performing the wafer acceptance test but before the wafer sort tests. The baking process eliminates any charges trapped inside the tunnel oxide layer within the silicon nitride read-only-memory.

[0037] Furthermore, the removal of trapped holes from the tunnel oxide layer of the wafer prevents any substantial loss of charges from the charge-trapping layer or even if a cell retention check is subsequently carried out. Ultimately, there is very little drop in the threshold voltage of the memory cell and the charge retention capacity of the

wafer (with silicon nitride read-only-memory therein) is greatly improved.

[0038] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.